

VARIABLE CLOCK CONFIGURATION FOR SWITCHED OP-AMP CIRCUITS

5 Background of the Invention:

Field of the Invention:

The invention relates to a circuit configuration in switched op-amp technology and to a method for clocking successive operational amplifier stages constructed in switched op-amp technology.

The switched op-amp technology has developed from the switched capacitor technology to be able to take into account the requirement for ever-lower supply voltages. The switched op-amp technology is used in the construction of filters and converters and is especially suitable for fields of application in which low power consumption is of importance. The field includes, for example, applications in the mobile radio field in which the load on the battery must be kept as low as possible.

Whereas the capacitors are switched on and off by clocked switches in the switched capacitor technology, the operational amplifiers are also switched on and off by a switching clock signal in the switched op-amp technology. Such a configuration results in considerable power saving.

In the prior art, two successive operational amplifier stages are operated with opposite clock pulses. A prior art non-overlapping two-phase clock is used for the clocking.

- 5 Accordingly, the operational amplifiers of the successive stages are never active at the same time. However, the clock configuration is selected such that each operational amplifier is switched on for approximately 50%.

Summary of the Invention:

It is accordingly an object of the invention to provide a variable clock configuration for switched op-amp circuits and a method for clocking successive operational amplifier stages constructed in switched op-amp technology, that overcomes the hereinafore-mentioned disadvantages of the heretofore-known devices and methods of this general type and that achieves a further reduction in the power consumption of switched op-amp circuits.

- 20 With the foregoing and other objects in view, there is provided, in accordance with the invention, a circuit configuration in switched op-amp technology including at least one switchable operational amplifier having an input and an output, at least one sampling capacitor connected to the
- 25 input, at least one integrating capacitor connected to the input and to the output, a clock generator producing at least

two non-overlapping switching-clock signals each having switching-clock phases including an on-phase and an off-phase; and a phase-variance device varying the switching-clock phases in which the first and second switching-clock signals are in the off-phase. The phase-variance device is connected to the clock generator. The at least two non-overlapping switching-clock signals include a first switching-clock signal and a second switching-clock signal. The clock generator controls charging of the sampling capacitor with the first switching-clock signal and switching the operational amplifier on and off with the second switching-clock signal.

The circuit configuration in switched op-amp technology according to the invention includes at least one switchable operational amplifier, at least one sampling capacitor that can be connected to the input of the operational amplifier, and at least one integration capacitor disposed between the input and the output of the operational amplifier.

At least two non-overlapping switching-clock signals are generated for controlling the circuit configuration. As long as one of the two switching-clock signals is at 1, the sampling capacitor is charged up by the input signal. During the phase, the other one of the two switching-clock signals is at 0 and the operational amplifier is in its switched-off state. At the end of the sampling phase, all switching-clock

signals are in a common off-phase. The other one of the two switching-clock signals then changes to 1 and, thus, switches on the operational amplifier. During the integration-phase that now starts, the operational amplifier, as the active component, transfers the charge of the sampling capacitor connected to its input to the integration capacitor. At the end of the integration-phase, both switching-clock signals are again at 0.

The circuit configuration according to the invention has a device or means for varying the switching-clock phases in which all switching-clock signals are in the off-phase. The configuration makes it possible to stretch the switching-clock phases in which both switching-clock signals are at 0, at the cost of the on-phases. It is only necessary to ensure that the sampling capacitor can be completely charged up by the input signal during the on-phase of one switching-clock signal and that the operational amplifier can settle sufficiently for the charge to be transferred to the integration capacitor during the on-phase of the other switching-clock signal.

Thus, the common off-phase of the two switching-clock signals can be extended up to the limit predetermined by the transient response, making it possible to use the potential for power saving to its full extent. The invention is, thus, particularly suitable for use in mobile transceivers

(mobiles), mobile Internet devices (WAP technology) but also for medical use (hearing aids, pacemakers etc.) in which a long life of the batteries used is of importance.

5 In particular, the invention makes it possible to adapt the length of the on- and off-phases individually to the Q factor of the operational amplifiers used. To take into consideration the influence of process spreads in the manufacture, analog circuits must be dimensioned such that they still meet the required specification even with disadvantageous process effects. In many cases, therefore, the behavior of an analog circuit is better than specified by the manufacturer. If the transient response of the operational amplifier used is better than specified, the potential can be exploited for saving power using the invention.

In accordance with another feature of the invention, it is an advantage if each of the switching-clock phases in which all  
20 switching-clock signals are in the off-phase is variable. Both the common off-phase that follows the on-phase of the first switching-clock signal and the common off-phase that follows the on-phase of the second switching-clock signal are extended. The process results in a uniform switching  
25 configuration. However, it is also possible to make the off-phase following the on-phase of the first switching-clock

signal and the off-phase following the on-phase of the second switching-clock signal be different lengths.

As an alternative, in accordance with another feature of the invention, it is possible to vary only every second one of the switching-clock phases in which all switching-clock signals are in the off-phase. In such a solution, in each case only the off-phase following the on-phase of the first switching-clock signal is extended or in each case only the off-phase following the on-phase of the second switching-clock signal is extended. Thus, every second common off-phase is in each case extended.

It is an advantage, in accordance with an added feature of the invention, if the duration of the switching-clock phases in which all switching-clock signals are in the off-phase can be varied in dependence on the transient response of the operational amplifier. To achieve maximum power saving, the on-phase must be selected to be just long enough for the operational amplifier to be able to settle. Once the transient has ended, the operational amplifier can be switched off.

In accordance with an additional feature of the invention, the duration of the switching-clock phases in which all switching-clock signals are in the off-phase can be varied in dependence

on the switching speed of the transistors. Because an operational amplifier is made of individual transistors, the transient response of the operational amplifier is essentially determined by the switching speed of the transistors. Thus, the transistor switching speed is an easily detectable measure of the transient response of the operational amplifier. The switching speed of the transistors can be used directly for determining the duration of the common off-phases: The faster the switching of the transistors, the longer the common off-phase can be selected to be and the greater the power savings.

It is an advantage, in accordance with yet another feature of the invention, if the circuit configuration includes a device or means for detecting the transistor switching speed connected to the operational amplifier. With such a device, the transistor switching speed can be detected individually on the substrate so that the length of the common off-phases can be matched to the Q factor of the operational amplifier used.

It is then an advantage, in accordance with yet a further feature of the invention, if the switching speed of n-channel FETs and/or of p-channel FETs can be detected separately. The process for producing n-type FETs and p-type FETs includes completely different process steps. As such, it is possible that n-type FETs and p-type FETs located on the same substrate differ considerably with regard to their switching speeds.

Depending on the internal circuitry of an operational amplifier, its transient response may be mainly determined by the behavior of the n-type FETs or of the p-type FETs. In such a case, it is recommended to detect the switching speed  
5 of the significant device type separately.

10  
11  
12  
13  
14  
15  
16  
17  
18  
19  
20  
21  
22  
23  
24  
25  
26  
27  
28  
29  
30  
31  
32  
33  
34  
35  
36  
37  
38  
39  
40  
41  
42  
43  
44  
45  
46  
47  
48  
49  
50  
51  
52  
53  
54  
55  
56  
57  
58  
59  
60  
61  
62  
63  
64  
65  
66  
67  
68  
69  
70  
71  
72  
73  
74  
75  
76  
77  
78  
79  
80  
81  
82  
83  
84  
85  
86  
87  
88  
89  
90  
91  
92  
93  
94  
95  
96  
97  
98  
99  
100  
101  
102  
103  
104  
105  
106  
107  
108  
109  
110  
111  
112  
113  
114  
115  
116  
117  
118  
119  
120  
121  
122  
123  
124  
125  
126  
127  
128  
129  
130  
131  
132  
133  
134  
135  
136  
137  
138  
139  
140  
141  
142  
143  
144  
145  
146  
147  
148  
149  
150  
151  
152  
153  
154  
155  
156  
157  
158  
159  
160  
161  
162  
163  
164  
165  
166  
167  
168  
169  
170  
171  
172  
173  
174  
175  
176  
177  
178  
179  
180  
181  
182  
183  
184  
185  
186  
187  
188  
189  
190  
191  
192  
193  
194  
195  
196  
197  
198  
199  
200  
201  
202  
203  
204  
205  
206  
207  
208  
209  
210  
211  
212  
213  
214  
215  
216  
217  
218  
219  
220  
221  
222  
223  
224  
225  
226  
227  
228  
229  
230  
231  
232  
233  
234  
235  
236  
237  
238  
239  
240  
241  
242  
243  
244  
245  
246  
247  
248  
249  
250  
251  
252  
253  
254  
255  
256  
257  
258  
259  
260  
261  
262  
263  
264  
265  
266  
267  
268  
269  
270  
271  
272  
273  
274  
275  
276  
277  
278  
279  
280  
281  
282  
283  
284  
285  
286  
287  
288  
289  
290  
291  
292  
293  
294  
295  
296  
297  
298  
299  
300  
301  
302  
303  
304  
305  
306  
307  
308  
309  
310  
311  
312  
313  
314  
315  
316  
317  
318  
319  
320  
321  
322  
323  
324  
325  
326  
327  
328  
329  
330  
331  
332  
333  
334  
335  
336  
337  
338  
339  
340  
341  
342  
343  
344  
345  
346  
347  
348  
349  
350  
351  
352  
353  
354  
355  
356  
357  
358  
359  
360  
361  
362  
363  
364  
365  
366  
367  
368  
369  
370  
371  
372  
373  
374  
375  
376  
377  
378  
379  
380  
381  
382  
383  
384  
385  
386  
387  
388  
389  
390  
391  
392  
393  
394  
395  
396  
397  
398  
399  
400  
401  
402  
403  
404  
405  
406  
407  
408  
409  
410  
411  
412  
413  
414  
415  
416  
417  
418  
419  
420  
421  
422  
423  
424  
425  
426  
427  
428  
429  
430  
431  
432  
433  
434  
435  
436  
437  
438  
439  
440  
441  
442  
443  
444  
445  
446  
447  
448  
449  
450  
451  
452  
453  
454  
455  
456  
457  
458  
459  
460  
461  
462  
463  
464  
465  
466  
467  
468  
469  
470  
471  
472  
473  
474  
475  
476  
477  
478  
479  
480  
481  
482  
483  
484  
485  
486  
487  
488  
489  
490  
491  
492  
493  
494  
495  
496  
497  
498  
499  
500  
501  
502  
503  
504  
505  
506  
507  
508  
509  
510  
511  
512  
513  
514  
515  
516  
517  
518  
519  
520  
521  
522  
523  
524  
525  
526  
527  
528  
529  
530  
531  
532  
533  
534  
535  
536  
537  
538  
539  
540  
541  
542  
543  
544  
545  
546  
547  
548  
549  
550  
551  
552  
553  
554  
555  
556  
557  
558  
559  
560  
561  
562  
563  
564  
565  
566  
567  
568  
569  
570  
571  
572  
573  
574  
575  
576  
577  
578  
579  
580  
581  
582  
583  
584  
585  
586  
587  
588  
589  
590  
591  
592  
593  
594  
595  
596  
597  
598  
599  
600  
601  
602  
603  
604  
605  
606  
607  
608  
609  
610  
611  
612  
613  
614  
615  
616  
617  
618  
619  
620  
621  
622  
623  
624  
625  
626  
627  
628  
629  
630  
631  
632  
633  
634  
635  
636  
637  
638  
639  
640  
641  
642  
643  
644  
645  
646  
647  
648  
649  
650  
651  
652  
653  
654  
655  
656  
657  
658  
659  
660  
661  
662  
663  
664  
665  
666  
667  
668  
669  
670  
671  
672  
673  
674  
675  
676  
677  
678  
679  
680  
681  
682  
683  
684  
685  
686  
687  
688  
689  
690  
691  
692  
693  
694  
695  
696  
697  
698  
699  
700  
701  
702  
703  
704  
705  
706  
707  
708  
709  
710  
711  
712  
713  
714  
715  
716  
717  
718  
719  
720  
721  
722  
723  
724  
725  
726  
727  
728  
729  
730  
731  
732  
733  
734  
735  
736  
737  
738  
739  
740  
741  
742  
743  
744  
745  
746  
747  
748  
749  
750  
751  
752  
753  
754  
755  
756  
757  
758  
759  
760  
761  
762  
763  
764  
765  
766  
767  
768  
769  
770  
771  
772  
773  
774  
775  
776  
777  
778  
779  
780  
781  
782  
783  
784  
785  
786  
787  
788  
789  
790  
791  
792  
793  
794  
795  
796  
797  
798  
799  
800  
801  
802  
803  
804  
805  
806  
807  
808  
809  
810  
811  
812  
813  
814  
815  
816  
817  
818  
819  
820  
821  
822  
823  
824  
825  
826  
827  
828  
829  
830  
831  
832  
833  
834  
835  
836  
837  
838  
839  
840  
841  
842  
843  
844  
845  
846  
847  
848  
849  
850  
851  
852  
853  
854  
855  
856  
857  
858  
859  
860  
861  
862  
863  
864  
865  
866  
867  
868  
869  
870  
871  
872  
873  
874  
875  
876  
877  
878  
879  
880  
881  
882  
883  
884  
885  
886  
887  
888  
889  
890  
891  
892  
893  
894  
895  
896  
897  
898  
899  
900  
901  
902  
903  
904  
905  
906  
907  
908  
909  
910  
911  
912  
913  
914  
915  
916  
917  
918  
919  
920  
921  
922  
923  
924  
925  
926  
927  
928  
929  
930  
931  
932  
933  
934  
935  
936  
937  
938  
939  
940  
941  
942  
943  
944  
945  
946  
947  
948  
949  
950  
951  
952  
953  
954  
955  
956  
957  
958  
959  
960  
961  
962  
963  
964  
965  
966  
967  
968  
969  
970  
971  
972  
973  
974  
975  
976  
977  
978  
979  
980  
981  
982  
983  
984  
985  
986  
987  
988  
989  
990  
991  
992  
993  
994  
995  
996  
997  
998  
999  
1000  
1001  
1002  
1003  
1004  
1005  
1006  
1007  
1008  
1009  
1010  
1011  
1012  
1013  
1014  
1015  
1016  
1017  
1018  
1019  
1020  
1021  
1022  
1023  
1024  
1025  
1026  
1027  
1028  
1029  
1030  
1031  
1032  
1033  
1034  
1035  
1036  
1037  
1038  
1039  
1040  
1041  
1042  
1043  
1044  
1045  
1046  
1047  
1048  
1049  
1050  
1051  
1052  
1053  
1054  
1055  
1056  
1057  
1058  
1059  
1060  
1061  
1062  
1063  
1064  
1065  
1066  
1067  
1068  
1069  
1070  
1071  
1072  
1073  
1074  
1075  
1076  
1077  
1078  
1079  
1080  
1081  
1082  
1083  
1084  
1085  
1086  
1087  
1088  
1089  
1090  
1091  
1092  
1093  
1094  
1095  
1096  
1097  
1098  
1099  
1100  
1101  
1102  
1103  
1104  
1105  
1106  
1107  
1108  
1109  
1110  
1111  
1112  
1113  
1114  
1115  
1116  
1117  
1118  
1119  
1120  
1121  
1122  
1123  
1124  
1125  
1126  
1127  
1128  
1129  
1130  
1131  
1132  
1133  
1134  
1135  
1136  
1137  
1138  
1139  
1140  
1141  
1142  
1143  
1144  
1145  
1146  
1147  
1148  
1149  
1150  
1151  
1152  
1153  
1154  
1155  
1156  
1157  
1158  
1159  
1160  
1161  
1162  
1163  
1164  
1165  
1166  
1167  
1168  
1169  
1170  
1171  
1172  
1173  
1174  
1175  
1176  
1177  
1178  
1179  
1180  
1181  
1182  
1183  
1184  
1185  
1186  
1187  
1188  
1189  
1190  
1191  
1192  
1193  
1194  
1195  
1196  
1197  
1198  
1199  
1200  
1201  
1202  
1203  
1204  
1205  
1206  
1207  
1208  
1209  
1210  
1211  
1212  
1213  
1214  
1215  
1216  
1217  
1218  
1219  
1220  
1221  
1222  
1223  
1224  
1225  
1226  
1227  
1228  
1229  
1230  
1231  
1232  
1233  
1234  
1235  
1236  
1237  
1238  
1239  
1240  
1241  
1242  
1243  
1244  
1245  
1246  
1247  
1248  
1249  
1250  
1251  
1252  
1253  
1254  
1255  
1256  
1257  
1258  
1259  
1260  
1261  
1262  
1263  
1264  
1265  
1266  
1267  
1268  
1269  
1270  
1271  
1272  
1273  
1274  
1275  
1276  
1277  
1278  
1279  
1280  
1281  
1282  
1283  
1284  
1285  
1286  
1287  
1288  
1289  
1290  
1291  
1292  
1293  
1294  
1295  
1296  
1297  
1298  
1299  
1300  
1301  
1302  
1303  
1304  
1305  
1306  
1307  
1308  
1309  
1310  
1311  
1312  
1313  
1314  
1315  
1316  
1317  
1318  
1319  
1320  
1321  
1322  
1323  
1324  
1325  
1326  
1327  
1328  
1329  
1330  
1331  
1332  
1333  
1334  
1335  
1336  
1337  
1338  
1339  
1340  
1341  
1342  
1343  
1344  
1345  
1346  
1347  
1348  
1349  
1350  
1351  
1352  
1353  
1354  
1355  
1356  
1357  
1358  
1359  
1360  
1361  
1362  
1363  
1364  
1365  
1366  
1367  
1368  
1369  
1370  
1371  
1372  
1373  
1374  
1375  
1376  
1377  
1378  
1379  
1380  
1381  
1382  
1383  
1384  
1385  
1386  
1387  
1388  
1389  
1390  
1391  
1392  
1393  
1394  
1395  
1396  
1397  
1398  
1399  
1400  
1401  
1402  
1403  
1404  
1405  
1406  
1407  
1408  
1409  
1410  
1411  
1412  
1413  
1414  
1415  
1416  
1417  
1418  
1419  
1420  
1421  
1422  
1423  
1424  
1425  
1426  
1427  
1428  
1429  
1430  
1431  
1432  
1433  
1434  
1435  
1436  
1437  
1438  
1439  
1440  
1441  
1442  
1443  
1444  
1445  
1446  
1447  
1448  
1449  
1450  
1451  
1452  
1453  
1454  
1455  
1456  
1457  
1458  
1459  
1460  
1461  
1462  
1463  
1464  
1465  
1466  
1467  
1468  
1469  
1470  
1471  
1472  
1473  
1474  
1475  
1476  
1477  
1478  
1479  
1480  
1481  
1482  
1483  
1484  
1485  
1486  
1487  
1488  
1489  
1490  
1491  
1492  
1493  
1494  
1495  
1496  
1497  
1498  
1499  
1500  
1501  
1502  
1503  
1504  
1505  
1506  
1507  
1508  
1509  
1510  
1511  
1512  
1513  
1514  
1515  
1516  
1517  
1518  
1519  
1520  
1521  
1522  
1523  
1524  
1525  
1526  
1527  
1528  
1529  
1530  
1531  
1532  
1533  
1534  
1535  
1536  
1537  
1538  
1539  
1540  
1541  
1542  
1543  
1544  
1545  
1546  
1547  
1548  
1549  
1550  
1551  
1552  
1553  
1554  
1555  
1556  
1557  
1558  
1559  
1560  
1561  
1562  
1563  
1564  
1565  
1566  
1567  
1568  
1569  
1570  
1571  
1572  
1573  
1574  
1575  
1576  
1577  
1578  
1579  
1580  
1581  
1582  
1583  
1584  
1585  
1586  
1587  
1588  
1589  
1590  
1591  
1592  
1593  
1594  
1595  
1596  
1597  
1598  
1599  
1600  
1601  
1602  
1603  
1604  
1605  
1606  
1607  
1608  
1609  
1610  
1611  
1612  
1613  
1614  
1615  
1616  
1617  
1618  
1619  
1620  
1621  
1622  
1623  
1624  
1625  
1626  
1627  
1628  
1629  
1630  
1631  
1632  
1633  
1634  
1635  
1636  
1637  
1638  
1639  
1640  
1641  
1642  
1643  
1644  
1645  
1646  
1647  
1648  
1649  
1650  
1651  
1652  
1653  
1654  
1655  
1656  
1657  
1658  
1659  
1660  
1661  
1662  
1663  
1664  
1665  
1666  
1667  
1668  
1669  
1670  
1671  
1672  
1673  
1674  
1675  
1676  
1677  
1678  
1679  
1680  
1681  
1682  
1683  
1684  
1685  
1686  
1687  
1688  
1689  
1690  
1691  
1692  
1693  
1694  
1695  
1696  
1697  
1698  
1699  
1700  
1701  
1702  
1703  
1704  
1705  
1706  
1707  
1708  
1709  
1710  
1711  
1712  
1713  
1714  
1715  
1716  
1717  
1718  
1719  
1720  
1721  
1722  
1723  
1724  
1725  
1726  
1727  
1728  
1729  
1730  
1731  
1732  
1733  
1734  
1735  
1736  
1737  
1738  
1739  
1740  
1741  
1742  
1743  
1744  
1745  
1746  
1747  
1748  
1749  
1750  
1751  
1752  
1753  
1754  
1755  
1756  
1757  
1758  
1759  
1760  
1761  
1762  
1763  
1764  
1765  
1766  
1767  
1768  
1769  
1770  
1771  
1772  
1773  
1774  
1775  
1776  
1777  
1778  
1779  
1780  
1781  
1782  
1783  
1784  
1785  
1786  
1787  
1788  
1789  
1790  
1791  
1792  
1793  
1794  
1795  
1796  
1797  
1798  
1799  
1800  
1801  
1802  
1803  
1804  
1805  
1806  
1807  
1808  
1809  
1810  
1811  
1812  
1813  
1814  
1815  
1816  
1817  
1818  
1819  
1820  
1821  
1822  
1823  
1824  
1825  
1826  
1827  
1828  
1829  
1830  
1831  
1832  
1833  
1834  
1835  
1836  
1837  
1838  
1839  
1840  
1841  
1842  
1843  
1844  
1845  
1846  
1847  
1848  
1849  
1850  
1851  
1852  
1853  
1854  
1855  
1856  
1857  
1858  
1859  
1860  
1861  
1862  
1863  
1864  
1865  
1866  
1867  
1868  
1869  
1870  
1871  
1872  
1873  
1874  
1875  
1876  
1877  
1878  
1879  
1880  
1881  
1882  
1883  
1884  
1885  
1886  
1887  
1888  
1889  
1890  
1891  
1892  
1893  
1894  
1895  
1896  
1897  
1898  
1899  
1900  
1901  
1902  
1903  
1904  
1905  
1906  
1907  
1908  
1909  
1910  
1911  
1912  
1913  
1914  
1915  
1916  
1917  
1918  
1919  
1920  
1921  
1922  
1923  
1924  
1925  
1926  
1927  
1928  
1929  
1930  
1931  
1932  
1933  
1934  
1935  
1936  
1937  
1938  
1939  
1940  
1941  
1942  
1943  
1944  
1945  
1946  
1947  
1948  
1949  
1950  
1951  
1952  
1953  
1954  
1955  
1956  
1957  
1958  
1959  
1960  
1961  
1962  
1963  
1964  
1965  
1966  
1967  
1968  
1969  
1970  
1971  
1972  
1973  
1974  
1975  
1976  
1977  
1978  
1979  
1980  
1981  
1982  
1983  
1984  
1985  
1986  
1987  
1988  
1989  
1990  
1991  
1992  
1993  
1994  
1995  
1996  
1997  
1998  
1999  
2000  
2001  
2002  
2003  
2004  
2005  
2006  
2007  
2008  
2009  
2010  
2011  
2012  
2013  
2014  
2015  
2016  
2017  
2018  
2019  
2020  
2021  
2022  
2023  
2024  
2025  
2026  
2027  
2028  
2029  
2030  
2031  
2032  
2033  
2034  
2035  
2036  
2037  
2038  
2039  
2040  
2041  
2042  
2043  
2044  
2045  
2046  
2047  
2048  
2049  
2050  
2051  
2052  
2053  
2054  
2055  
2056  
2057  
2058  
2059  
2060  
2061  
2062  
2063  
2064  
2065  
2066  
2067  
2068  
2069  
2070  
2071  
2072  
2073  
2074  
2075  
2076  
2077  
2078  
2079  
2080  
2081  
2082  
2083  
2084  
2085  
2086  
2087  
2088  
2089  
2090  
2091  
2092  
2093  
2094  
2095  
2096  
2097  
2098  
2099  
2100  
2101  
2102  
2103  
2104  
2105  
2106  
2107  
2108  
2109  
2110  
2111  
2112  
2113  
2114  
2115  
2116  
2117  
2118  
2119  
2120  
2121  
2122  
2123  
2124  
2125  
2126  
2127  
2128  
2129  
2130  
2131  
2132  
2133  
2134  
2135  
2136  
2137  
2138  
2139  
2140  
2141  
2142  
2143  
2144  
2145  
2146  
2147  
2148  
2149  
2150  
2151  
2152  
2153  
2154  
2155  
2156  
2157  
2158  
2159  
2160  
2161  
2162  
2163  
2164  
2165  
2166  
2167  
2168  
2169  
2170  
2171  
2172  
2173  
2174  
2175  
2176  
2177  
2178  
2179  
2180  
2181  
2182  
2183  
2184  
2185  
2186  
2187  
2188  
2189  
2190  
2191  
2192  
2193  
2194  
2195  
2196  
2197  
2198  
2199  
2200  
2201  
2202  
2203  
2204  
2205  
2206  
2207  
2208  
2209  
2210  
2211  
2212  
2213  
2214  
2215  
2216  
2217  
2218  
2219  
2220  
2221  
2222  
2223  
2224  
2225  
2226  
2227  
22



inputs receiving an edge signal delayed through the inverter chain, and an XNOR gate with XNOR inputs, one of the XNOR inputs receiving an undelayed edge signal and another of the XNOR inputs receiving an edge signal delayed through the inverter chain.

Quite generally, it is an advantage, in accordance with yet an additional feature of the invention, if the device for detecting the transistor switching speed generates pulses, the duration of which characterizes the switching speed of the transistors. The duration of such pulses can be detected accurately with the aid of counter and timer chips and can be used as the basis for digital closed-loop control.

It is of advantage, in accordance with again another feature of the invention, to adjust the duration of the switching-clock phases in which all switching-clock signals are in the off-phase in dependence on the duration of the measuring circuit pulses. As the switching of the transistors becomes faster, the pulses occurring at the output of the measuring circuit become shorter and the on-phases that can be selected also become shorter. The common off-phases of the switching-clock signals can be correspondingly extended.

In accordance with again a further feature of the invention, the duration of the switching-clock phases in which all

switching-clock signals are in the off-phase can be adjusted in a number of predetermined steps. The embodiment is based on the concept that a large proportion of the power saving can be achieved already with a relatively coarse adjustment of the duration of the on-phases and of the common off-phase. As such, it makes sense to adapt the duration of the switching-clock phases in which all switching-clock signals are in the off-phase only in steps. The adaptation can be achieved with little circuit expenditure.

In accordance with again an added feature of the invention, the clock generator or means for clock generation and the device for varying the switching-clock phases in which all switching-clock signals are in the off-phase are preferably implemented by a programmable clock generator. In a programmable clock generator, the lengths of the individual switching-clock phases are represented digitally and are converted into corresponding switching-clock signals by counter and timer circuits. The duration of the individual switching-clock phases can be reprogrammed in a simple manner.

As an alternative, it is an advantage, in accordance with again an additional feature of the invention, if an external squarewave generator and a divider circuit implement the clock generator and the device for varying the switching-clock phases in which all switching-clock signals are in the off-

phase. In such a configuration, the divider circuit generates the at least two switching-clock signals from the squarewave signal. The generation makes it possible to find out with little external circuit expenditure what the magnitude of the spread of the transient response is with a certain filter or converter circuit and whether or not there is still potential for power saving. The duty ratio of the squarewave signal can be adjusted at the external squarewave generator. The common off-phase of the switching-clock signals can be varied by the duty ratio.

It is an advantage, in accordance with still another feature of the invention, if the circuit configuration is implemented in fully differential circuit technology. In mobile radio technology applications in particular, differential construction of the signal lines makes it possible to eliminate interference effectively.

With the objects of the invention in view, there is also provided a method for clocking successive operational amplifier stages constructed in switched op-amp technology, including the steps of generating at least two non-overlapping switching-clock signals, switching a first operational amplifier on and off with a first signal of the two switching-clock signals, switching a second operational amplifier on and off with a second signal of the switching-clock signals, and

varying switching-clock phases in which the operational amplifiers are switched off.

In the method according to the invention for clocking  
5 successive operational amplifier stages constructed in  
switched op-amp technology, at least two non-overlapping  
switching-clock signals are generated in a first step, the  
first switching-clock signal switching a first operational  
amplifier on and off, and the second switching-clock signal  
switching a second operational amplifier on and off. In a  
second step, the phases of the switching-clock signals in  
which all operational amplifiers are switched off are varied.

Introducing a controllable common off-phase makes it possible  
to reduce the on times of the operational amplifier to the  
necessary degree so that the power consumption of the circuit  
can be restricted to a minimum.

In accordance with still a further mode of the invention, each  
20 of the switching-clock phases in which the operational  
amplifiers are switched off is varied.

In accordance with still an added mode of the invention, each  
second one of the switching-clock phases in which the  
25 operational amplifiers are switched off is varied.

In accordance with still an additional mode of the invention, a duration of the switching-clock phases in which the operational amplifiers are switched off dependent on a transient response of the operational amplifiers is varied.

5

In accordance with another mode of the invention, a duration of the switching-clock phases in which the operational amplifiers are switched off dependent on a switching speed of transistors of the operational amplifiers is varied.

In accordance with a further mode of the invention, at least one of a switching speed of n-channel FETs and a switching speed of p-channel FETs are separately detected.

In accordance with an added mode of the invention, at least one of a switching speed of n-channel FETs and a switching speed of p-channel FETs are separately detected.

In accordance with an additional mode of the invention, a duration of the switching-clock phases in which the operational amplifiers are switched off is adjusted in a number of predetermined steps.

In accordance with yet another mode of the invention, the non-overlapping switching-clock signals are generated with a programmable clock generator.

In accordance with yet a further mode of the invention, the non-overlapping switching-clock signals are generated with an external squarewave generator and a divider circuit.

5

In accordance with a concomitant mode of the invention, the switching-clock phases in which the operational amplifiers are switched off are varied by adjusting a duty ratio of a squarewave signal from the squarewave generator.

Other features that are considered as characteristic for the invention are set forth in the appended claims.

Although the invention is illustrated and described herein as embodied in a variable clock configuration for switched op-amp circuits, it is, nevertheless, not intended to be limited to the details shown because various modifications and structural changes may be made therein without departing from the spirit of the invention and within the scope and range of equivalents of the claims.

20

The construction and method of operation of the invention, however, together with additional objects and advantages thereof, will be best understood from the following description of specific embodiments when read in connection with the accompanying drawings.

25

Brief Description of the Drawings:

FIG. 1 is a schematic circuit diagram of a prior art circuit in switched op-amp technology including a number of  
5 operational amplifier stages;

FIG. 2A is a block and schematic circuit diagram of a prior art circuit for generating a non-overlapping two-phase clock;

FIG. 2B is a timing diagram illustrating the input clock signal and the even and odd switching-clock signals generated by the circuit according to FIG. 2A;

FIG. 3 is a block circuit diagram of a clock generating unit according to the invention including a circuit for determining the transistor switching speed;

FIG. 4 is a block and schematic circuit diagram of an example circuit for determining the gate delay and the transistor  
20 switching speed for use in the clock generating unit according to FIG. 3;

FIG. 5A is a timing diagram illustrating the input clock signal and the output signal of the circuit of FIG. 4 for a  
25 case of short gate delays;

FIG. 5B is a timing diagram illustrating a variation with time of the even and odd switching-clock signals generated by the clock generating unit according to FIG. 3 for the case of short gate delays;

5

FIG. 6A is a timing diagram illustrating a representation of the input clock signal and of the output signal of the circuit shown in FIG. 4 for a case of long gate delays;

FIG. 6B is a timing diagram illustrating a variation with time of the even and odd switching-clock signals generated by the clock generating unit according to FIG. 3 for the case of long gate delays;

FIG. 7 is a schematic circuit diagram of a circuit providing for the separate determination of the switching speed of n-channel MOSFETs according to the invention; and

FIG. 8 is a timing diagram illustrating an overview of the clock signals of an external clock generating unit according to the invention in which the even clock signal and the odd clock signal are generated from a squarewave signal by a divider circuit.

25



Description of the Preferred Embodiments:

In all the figures of the drawing, sub-features and integral parts that correspond to one another bear the same reference symbol in each case.

5

Referring now to the figures of the drawings in detail and first, particularly to FIG. 1 thereof, there is shown a prior art switched op-amp circuit that includes two operational amplifier stages. The operational amplifier 1, the sampling capacitor 2, the integration capacitor 3, and the capacitor 4 form the first operational amplifier stage. The second operational amplifier stage includes the operational amplifier 5, the sampling capacitor 6, the integration capacitor 7, and the capacitor 8. The various switches shown in FIG. 1 are switched on and off by two non-overlapping switching-clock signals that will be called even and odd switching-clock signals in the text that follows. Before discussing the operation of the circuit shown in FIG. 1 in greater detail, the generation of these two switching-clock signals will be explained with reference to FIGS. 2A and 2B.

10  
11  
12  
13  
14  
15  
16  
17  
18  
19  
20

FIG. 2A illustrates a prior art clock generator for generating a non-overlapping two-phase clock. A rectangular input clock signal 21 having the frequency  $f_{clk}$  is applied to the input of the circuit. The variation with time of the input clock signal 21 is shown in FIG. 2B.

25

The input clock signal 21 is present, on one hand, at the input of the inverter 22 and also at an input of the second NOR gate 24. The output of the inverter 22 is connected to an input of the first NOR gate 23. At the output of the NOR gate 23, the output signal 25 is present that is delayed by the two inverters 26. At the output of the inverter chain, the even switching-clock signal 27 can be picked up, the variation with time of which is shown in FIG. 2B. The even switching-clock signal 27 is connected to the second input of the second NOR gate 24, at the output of which the output signal 28 appears. The output signal 28 is delayed by the two inverters 29 and, at the output of the inverter chain, the odd switching-clock signal 30 can be picked up, the variation of time of which is also shown in FIG. 2B. The odd switching-clock signal 30 is supplied to the second input of the first NOR gate 23.

The comparison of the variation of the even switching-clock signal 27 and of the odd switching-clock signal 30 by referring to FIG. 2B shows that the odd switching-clock signal 30 is in each case switched off during the on-phase of the even switching-clock signal 27. In addition, both switching-clock signals are in a common off-phase between the on-phase of the even switching-clock signal 27 and the on-phase of the odd switching-clock signal 30 during the period  $\delta$ . It is, therefore, called a "non-overlapping two-phase clock".

Each of the switches shown in FIG. 1 is now switched on and off by the even switching-clock signal or by the odd switching-clock signal. Next to each switch, the switching clock by which it is clocked is noted.

Firstly, the first operational amplifier stage will now be considered during the on-phase of the even switching clock. The switches 9 and 10 are closed, therefore, whereas the switches 11, 12, 13 and 14 are open. The operational amplifier 1 is, therefore, inactive in such a phase. The input signal IN is present at one terminal of the sampling capacitor 2 and the other terminal is connected to VSS. The sampling capacitor 2 is, therefore, charged up by the input signal. The capacitor 4 is connected to VSS and VDD through the switches 9 and 10 and is, therefore, charged up by the supply voltage. The on-phase of the even switching-clock signal is followed - after a short common off-phase of both switching-clock signals - by the on-phase of the odd switching-clock signal. During such a phase, the switches 9 and 10 are open whereas the switches 11, 12, 13 and 14 are closed. Therefore, the operational amplifier 1 is switched on in the phase. One terminal of the sampling capacitor 2 is connected to VDD through the switch 12. The other terminal of the capacitor 2 is connected to the inverting input of the operational amplifier 1 through the switch 13. The capacitor

4 that is connected to VSS through the switch 14 in the phase additionally couples in a constant charge that produces a type of DC shift. The injected charge makes it possible to achieve an approximate potential VSS at the inverting input. The  
5 operational amplifier 1, as the active component, now attempts to correct its output to such an extent that the difference between the input voltages becomes zero. Therefore, the operational amplifier 1 attempts to bring the inverting input to VSS potential. As a result, precisely the charge quantity that has been sampled at the sampling capacitor 2 is transferred to the integration capacitor 3.

The second operational amplifier stage is operated in the opposite phase to the first one. Still being considered is the on-phase of the odd switching clock in which the operational amplifier 1 is active. The switches 15 and 16 of the second op-amp stage are closed and that is why the output of the operational amplifier 1 charges up the sampling capacitor 6 belonging to the second operational amplifier  
20 stage. Thus, the integration-phase of the first operational amplifier stage and the sampling phase of the second operational amplifier stage are taking place at the same time.

In the subsequent switching-clock phase, the charge quantity  
25 sampled at the sampling capacitor 6 is transferred to the integration capacitor 7. During such integration-phase of the

second operational amplifier stage, the first operational amplifier stage is already back in the sampling phase.

The switching clock configuration shown in FIG. 2B is modified by the invention such that the on times of the operational amplifiers are shortened and, thus, a power saving is achieved. The hardware according to the invention is illustrated in FIG. 3. A programmable clock generator 31 is supplied with a squarewave input clock signal 32 having the frequency  $f_{clk}$ . A circuit 33 for determining the transistor switching speed determines the switching speed of the transistors that is significant for the transient response of the operational amplifiers. A pulse signal 34 characteristic of the switching speed is supplied to the programmable clock generator 31 and taken into consideration in the generation of the even switching-clock signal 35 and of the odd switching-clock signal 36. The faster the switching of the devices are, the shorter the on-phases of the operational amplifiers can be.

FIG. 4 illustrates an example for a circuit 33 for determining the transistor switching speed. The input clock signal 37 is present at the first input of the XOR gate 40. At the second input of the XOR gate 40, the delayed and inverted clock signal 39 is present that is obtained from the input clock signal 37 by an odd number of inversions (FIG. 4 shows three

inverters 38). If the input clock signal 37 is at 0, the signal 39 assumes the value 1 and the output signal 41 of the XOR gate 40 assumes the value 1. If the input clock signal 37 changes from 0 to 1, the new value 1 is immediately available at the first input of the XOR gate 40. The signal 39 only changes to the new value 0 after a certain time delay that is determined by the gate delay of the three inverters 38. During a period that is characteristic of the gate delay, the output signal 41 is, therefore, at 0 and then it assumes the value 1.

The duration of the pulses in the output signal 41 represents a measure of the switching speed of the transistors of the substrate. The measurement makes it possible to detect the effect of process spreads on the transistor switching speed directly on the chip and to take it into consideration during the clock generation. Instead of the XOR gate, an XNOR gate can also be used for determining the switching speed of the transistors.

FIG. 5A illustrates the variation with time of the input clock signal 37 and of the output signal 41 of the XOR gate 40.

When the input clock signal 37 changes from 1 to 0, a falling signal edge 42 is obtained that triggers a pulse 43 with a pulse width  $t_D$  in the output signal 41. During the pulse period  $t_D$ , the output signal 41 assumes the value 0.

When the input clock signal 37 changes from 0 to 1, a rising signal edge 44 is obtained that also triggers a pulse 45 of length  $t_D$ . The pulses 43, 45 shown in FIG. 5A are short and the corresponding values of  $t_D$  are low. Accordingly, the inverters 38 only produce a slight signal delay, which allows a high switching speed of the transistors and a short transient response of the operational amplifiers to be inferred.

The pulse signal 41 is supplied to the programmable clock generator that digitizes the period of the pulses 43, 45 and uses them for calculating the switching clock configuration. For the case of a short pulse duration  $t_D$  shown in FIG. 5A, the switching clock signals generated by the programmable clock generator, the even switching-clock signal 46, and the odd switching-clock signal 47 are shown in FIG. 5B. Because of the fast transient response of the operational amplifiers, only short on-phases 48, 49 are required.

The switching clock phases 50, 51, in which both switching-clock signals 46 and 47 are in the off-phase, can be correspondingly extended. In the prior art clock configuration shown in FIG. 2B, the common off-phases had the period  $\delta$ . In the clock configuration shown in FIG. 5B, however, the duration of the common off-phases has been

increased to  $\delta + t_a$ . The operational amplifiers are only switched on until the transient is finished. During the common off-phases, all operational amplifiers are inactive.

5 FIG. 6A shows the input clock signal 52 and the output signal 53 of the XOR gate 40 for the case of transistors switching slowly or for long gate delays. The falling signal edge 54 causes a pulse 55 of duration  $t_D$  in the output signal 53 and the rising signal edge 56 correspondingly causes a pulse 57 of duration  $t_D$ . In the example shown in FIG. 6A, the transistors only have a low switching speed. The inverters 38, therefore, delay the signal considerably and the delay leads to a long pulse duration  $t_D$ , making it possible to infer a slow transient response of the operational amplifiers.

FIG. 6B shows the variation with time of the associated switching-clock signals, the even switching-clock signal 58 and the odd switching-clock signal 59. Because of the slow transient response of the operational amplifiers, the on-phases 60, 61 of the two switching-clock signals must be  
20 selected to be long. Accordingly, the common off-phase 62 of the switching-clock signals must be reduced to the minimum period  $\delta$ . Accordingly,  $t_a$  is set to be  $= 0$ .



The programmable clock generator maps the pulse duration  $t_D$  onto the duration of the common off-phase  $\delta + t_a$ , a small value of  $t_D$  being mapped onto a large value of  $\delta + t_a$  and a large value of  $t_D$  being mapped onto a small value of  $t_a$ . As such, the switching clock configuration can be adapted to the switching speed of the transistors such that the power saving is at a maximum.

FIG. 7 illustrates an embodiment of the circuit 33 for determining the transistor switching speed that selectively detects the switching characteristic of n-type MOSFETs. The use of such a circuit is recommended if the transient response of the operational amplifiers used is mainly determined by the characteristics of the transistors of the n-type. The circuit includes the p-type MOSFETs 65, 66, 67 and the n-type MOSFETs 68, 69, 70, 71, 72, 73. The current through the FETs depends on the width/length ratio (W/L) of the respective FET. In the example illustrated in FIG. 7, the p-type FETs 65, 66, 67 and the n-type FETs 68, 69, 70 have a large W/L. The n-type FETs 71, 72, 73, the W/L ratio of which is much lower than that of the other devices, therefore, have a current-limiting effect.

When the input signal 63 changes to VSS, the p-type FET 65 is gated on. The gate of the n-type MOSFET 69 is then at VDD and, if VBIAS has been suitably selected, the n-type FET 72 is

also conducting. The potential VSS can then be switched through to the gate of the p-type FET 67. The p-type FET 67 places an input of the XOR gate 64 at VDD. Because of the low value of W/L in the case of the n-type FET 72, in comparison with the W/L values of the FETs 65, 67, 69, the total delay is essentially determined by the n-type FET 72. When the input signal 63 changes to VDD, in contrast, the total delay essentially depends on the switching speed of the n-type FETs 71 and 73. In every case, the total delay is, therefore, mainly determined by the n-type FETs having a small W/L.

FIG. 8 illustrates a method of how the clock configuration according to the invention can be generated externally by a squarewave generator and a divider circuit. The squarewave generator supplies a squarewave signal 74 having the frequency ( $2 f_{clk}$ ). From the squarewave signal 74, the even switching-clock signal 75 and the odd switching-clock signal 76, which each have a period of  $\frac{1}{f_{clk}}$ , are derived by a divider circuit.

The duration of the common off-phase in which both switching-clock signals are equal to 0 can be adjusted by varying the duty ratio of the squarewave signal. The duty ratio of the squarewave signal 74 is 1/2 whereas the duty ratio of the squarewave signal 77 is 1/4. The squarewave signal 78 has a duty ratio of 3/4. The values of  $\delta + t_a$  that belong to the

[illegible]